

REMARKS/ARGUMENTS

Figures 2 and 3 submitted on January 10, 2006 were objected because the hand drawn features were allegedly illegible. As such, newly amended Figures 2 and 3 in compliance with 37 CFR 1.121(d) and 37 CFR 1.83(p) are submitted and withdrawal of the objection is earnestly requested.

Claim rejections 35 U.S.C. § 101

Claims 7, 8 and 19 were rejected, under 35 U.S.C. §101, because the claimed invention were allegedly directed to non-statutory subject matter. The Applicant has respectfully amended Claims 7, 8 and 19. The Applicant respectfully submits that Claims 7, 8 and 19 are directed to statutory subject matter in compliance with 35 U.S.C. §101, and withdrawal of the rejection is earnestly solicited.

Claim rejections 35 U.S.C. § 112, Second Paragraph

Claims 7, 8 and 19 were rejected, under 35 U.S.C. §112, Second Paragraph for allegedly failing to particularly point out and distinctly claim the subject matter of the invention. The Applicant has respectfully amended Claims 7, 8 and 19. Accordingly, the Applicant respectfully submits that Claims 7, 8 and 19 particularly point out and distinctly claim the subject matter of the invention in

compliance with 35 U.S.C. §112, Second Paragraph. As such, withdrawal of the rejection is earnestly solicited.

Claim rejections
35 U.S.C. § 103

Claims 1-2, 5-11, 13-16 and 18-20 were rejected, under 35 U.S.C. §103, as being allegedly unpatentable over US Pat. No. 5,357,626 (hereinafter Johnson) in view of US Pat. No. 6,366,878 (hereinafter Grunert) and further yet in view of US Pat. No. 4,176,258 (hereinafter Jackson). The Applicant respectfully traverses in view of the following.

Independent Claim 1 recites a limitation whereby a microcontroller is installed on a test circuit, as claimed. Moreover, independent Claim 1 recites a limitation whereby an ICE is coupled to a computer system, as claimed. Independent Claim 1 further recites a limitation whereby the microcontroller and the ICE run the microcontroller code in lock step by executing the same instructions using the same clocking signals, as claimed. Independent Claim 1 also recites a limitation whereby an interface enables data transmission between the test circuit and the computer system, as claimed. Moreover, independent Claim 1 recites a limitation whereby the computer system separate from the ICE is configured to compare a content of the first memory against a content of the second memory to verify the lock step, as claimed.

Johnson discloses a first processor and a second processor configured for executing instructions stored externally in the external memory (see Johnson, col. 5, lines 12-14 and see Figure 1) and an in circuit emulation to verify the execution by the first and the second processor (see Johnson, col. 3, lines 54-56). Johnson is silent regarding installation of the processors. Accordingly, Johnson fails to teach or suggest that a microcontroller is installed on a test circuit, as claimed.

Moreover, the rejection asserts that the second processor and the in circuit emulator (see Johnson, Figure 1, elements 14, 15 and 18) forms the ICE, as claimed. The rejection also asserts that the first processor (see Johnson, Figure 1, elements 12 and 13) forms the microcontroller, as claimed. However, the rejection fails to show an ICE coupled to a computer system, as claimed. Accordingly, Johnson fails to teach or suggest an ICE coupled to a computer system, as claimed.

The rejection relies on the bus 34 (see Figure 1, element 32) to show the interface, as claimed. As Applicant understands, the rejection seems to suggest that since Johnson does not disclose that the bus 34 (see Johnson, Figure 1 element 34) prevents data transmission, it must therefore enable data transmission between the test circuit and the computer system, as claimed. The Applicant respectfully reminds the Examiner that omission of a teaching in a

reference does not necessarily teach the opposite of that teaching, as seems to be suggested by the rejection. Moreover, the Applicant respectfully reminds the Examiner that to establish a *prima facie* case of obviousness the prior art reference (or references when combined) must teach or suggest all the claim limitations (see *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) and see MPEP 2100-126). Therefore, it is improper to rely on Johnson failing to disclose that the bus 34 prevents data transmission to show that it somehow enables data transmission between the test circuit and the computer system, as claimed by the present embodiment. Accordingly, Johnson fails to explicitly teach or suggest an interface enables data transmission between the test circuit and the computer system, as claimed.

The rejection admits that the Johnson fails to teach or suggest that the processors are microcontrollers, as claimed. The rejection relies on Grunert to remedy this failure. The rejection asserts that Grunert teaches two microcontrollers operating in lock step. The Applicant respectfully disagrees that Grunert teaches two microcontroller operating in lock step for the following reasons.

Grunert discloses one microcontroller operating as a master and another microcontroller operating as a slave and a clock synchronizing the two microcontrollers (see Grunert, col. 4, lines 26-39 and col. 2, lines 58-59). The

teaching by Grunert does not necessarily teach or suggest operating in lock step by executing the same instructions using the same clocking signals, as claimed.

For example, operating as a master and a slave and having a clock synchronizing the master and slave is to clock the two microcontrollers two cycles apart. Therefore, at the time of the invention, a person of ordinary skill in the art would not have been motivated to replace the processors disclosed in Johnson with microcontrollers disclosed in Grunert to arrive at the claimed embodiment.

The rejection admits that the combination of Johnson and Grunert fails to teach or suggest comparing a contents of the first memory against a content of the second memory to verify lock step operation, as claimed. The rejection relies on Jackson to remedy this failure. The Applicant respectfully traverses in view of the following.

Jackson discloses that redundant checking systems are well known in prior art (see Jackson, col. 1, lines 11-12). Jackson further discloses that an error checking logic circuit is fabricated on each of a number of chips such that the data generated on all but of one the chips is checked against data generated from the other chip (see Jackson, col. 1, lines 46-66). Accordingly, the checking logic circuit according to Jackson is an integral part of each chip. Accordingly, Jackson fails to teach or suggest a computer system separate from the ICE

configured to compare a content of the first memory against a content of the second memory to verify the lock step, as claimed.

Accordingly, the combination of Johnson, Grunert and further yet Jackson fails to render independent Claim 1 obvious, under 35 U.S.C. 103. Independent Claims 9 and 15 recite limitations similar to that of independent Claim 1 discussed above and are patentable for similar reasons. Dependent claims are patentable by virtue of their dependency.

Moreover, independent Claim 9 recites initializing a first memory of an ICE and a second memory of a microcontroller with microcontroller test code, as claimed. Independent Claim 9 further recites reporting an error and saving an execution history using a trace buffer if lock step execution is not verified, and continuing execution of the microcontroller test code if lock step execution is verified, as claimed.

The Applicant wishes to respectfully remind the Examiner that to establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; there must be a reasonable expectation of success and the prior art reference (or references when combined) must teach or suggest all the claim

limitations (see MPEP 2100-126). Moreover, Applicant wishes to respectfully remind the Examiner that “the examiner should set forth in the Office action: (A) the relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate” and “(B) the difference or differences in the claim over the applied reference(s)” (MPEP §706.02(j)). Accordingly, the Applicant respectfully submits that the rejection fails to establish a *prima facie* case of obviousness. As such, independent Claim 9 is patentable.

Regarding Claim 6, the rejection relies on Johnson disclosing that the first processor and second processor are coupled in master/slave configuration to permit the second processor to duplicate the instructions performed by the first processor (see Johnson, col. 3, lines 57-62). The Applicant does not understand a master/slave configuration to necessarily have a program counter wherein lock step execution is maintained by maintaining the program counters in lock step, as claimed.

Regarding Claims 7, 8 and 19 the rejection asserts that Jackson teaches comparing the outputs of the microcontroller processors to verify lock step operation. The Applicant respectfully submits the Jackson fails to teach or suggest displaying a content of memory, or displaying the state of CPUs capable of comparison for consistency when execution of the microcontroller is halted, as claimed.

Claim 14 was rejected under the same rationale as Claims 7, 8 and 19. The Applicant respectfully submits that Jackson fails to teach or suggest halting the execution when a breakpoint is encountered, and verifying lock step while execution is halted, as claimed.

As such, allowance of Claims 1-2, 5-11, 13-16 and 18-20 is earnestly solicited.

Claims 3, 12 and 17 were rejected as being allegedly unpatentable under 35 U.S.C. 103(a) over Johnson in view of Grunert and further in view of Jackson, as applied to Claims 1, 9 and 15 above, and further in view of Barnett (U.S. Patent No. 6,173,419) (hereinafter Barnett). The Applicant respectfully traverses the rejections.

Dependent Claims 3, 12 and 17 include the limitations of their respective independent claims. The Applicant does not understand Barnett to remedy failures of Johnson, Grunert and Jackson as discussed above. Thus, the cited combination does not render Claims 3, 12 and 17 obvious, under 35 U.S.C. 103(a). As such, allowance of Claims 3, 12 and 17 is earnestly solicited.

Claim 4 was rejected as being allegedly unpatentable, under 35 U.S.C. 103(a), over Johnson in view of Grunert and further in view of Jackson, and further in view of "State of the Art" by Stan Augarten, published 1983 (Augarten). The Applicant respectfully traverses the rejection.

Claim 4 depends from independent Claim 1 and includes the limitations of independent Claim 1. The Applicant does not understand Augarten to remedy failures of Johnson, Grunert and Jackson as discussed above. Thus, the cited combination does not render Claim 4 obvious, under 35 U.S.C. 103(a). As such, allowance of Claim 4 is earnestly solicited.

For the above reasons, the Applicant requests reconsideration and withdrawal of these rejections under 35 U.S.C. 101, 35 U.S.C. 112, Second Paragraph, and 35 U.S.C. §103.

CONCLUSION

In light of the above listed remarks, reconsideration of the rejected Claims 1-20 is requested. Based on the arguments presented above, it is respectfully submitted that Claims 1-20 overcome the rejections of record and, therefore, allowance of Claims 1-20 is earnestly solicited.

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